In the Specification:

Please replace the first paragraph of page 8 with the following new paragraph:

The physical port 220 has the address constant indicating the starting address of the memory-mapped device. The autowait (AWAIT) port 225 is a constant flag. When the AWAIT flag is high , one wait state is automatically generated to indicate to a device reading this address that it is going to take an additional bus clock cycle to get the data out of the memory mapped device. When the flag is low, there is no wait state. In another embodiment, the AWAIT port 225 can be configured to be multiple bits wide to enable encoding of additional wait states. The BUSCLK port receives clock signals from a bus coupled to the halfword selector data access primitive. The SIM port is a bi-directional port connected to the system bus functional model during simulation, allowing the socket primitives to be simulated in the context of various bus transactions. The SYMBOLIC port receives a symbolic address that is part of an address space. One skilled in the art would recognize that other wait states beyond those asserted by the data access primitive may be asserted by other logic in the design, depending on the needs of the design.

Please replace the second paragraph of page 8 with the following new paragraph:

Figure 3 is an exemplary diagram of another halfword selector data access primitive. The data access primitive in **Figure 3** is referred to herein as "HALFSELH" data access primitive. The ports in the HALFSELH data access primitive have the same function as for the HALFSEL data access primitive ports described above with respect to

Figure 2. The HALFSELH data access primitive is a restricted data access primitive because it can be used to connect a halfword-, or a word-addressable half-word entity to the data bus. The HALFSELH can not be used to address a byte of the half-word entity, which is different from the fully addressable HALFSEL data access primitive. The write-select (WRSEL) port 305 has one line which is shared by both bytes of the halfword. During a halfword or word write transaction, the line goes high when there is an address match. The read-select (RDSEL) port 308 has one line and goes high during a read transaction when the address matches. The HALFSELH data access primitive includes a data write port (DW) 310 and a data read port (DR) 315.

Please replace the third paragraph of page 8 with the following new paragraph:

Figure 4 is an exemplary diagram of byte selector data access primitive. The data access primitive in **Figure 4** is referred to herein as "BYTESEL" data access primitive. The ports in the BYTESEL data access primitive have the same function as the HALFSEL data access primitive ports described above with respect to **Figure 2.** The BYTESEL data access primitive is a fully addressable data access primitive because it can be used to connect a one-byte entity to the data bus. The BYTESEL data access primitive is very similar to the HALFSEL data access primitive, except that the write-select (WRSEL) port 405 and the read-select (RDSEL) 408 each has one line (bit) instead of two lines. The BYTESEL data access primitive also differs from the HALFSEL data access primitive in that it matches only a single byte rather than two bytes.